



EV182656601

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Application Serial Number ..... 09/292,132  
Filing Date ..... April 14, 1999  
Inventor ..... Salman Akram et al.  
Assignee ..... Micron Technology, Inc.  
Group Art Number ..... 2812  
Examiner ..... S. Mulpuri  
Attorney's Docket No. .... MI22-1171  
Title:     Methods of Forming a Transistor Gate

**SUPPLEMENTAL INFORMATION DISCLOSURE STATEMENT**


Reference -- See Attached Form PTO-1449

The attached form PTO-1449 is submitted in compliance with 37 CFR §1.56. No admission is made regarding whether the submitted reference is prior art.

Dated: 1-02-03

Attorney:

Respectfully submitted,

  
D. Brent Kenady  
Reg. #40,045

RECEIVED  
AUG - 4 2003  
TECHNOLOGY CENTER 2800

Form PTO-1449


  
 LIST OF ART CITED BY APPLICANT

(Use several sheets if necessary)

U.S. DEPARTMENT OF COMMERCE  
PATENT AND TRADEMARK OFFICEATTY. DOCKET NO.  
MI22-1171SERIAL NO.  
09/292,132APPLICANT  
Salman Akram et al.FILING DATE  
April 14, 1999GROUP  
2312

## U.S. PATENT DOCUMENTS

*Examiner Initial		Document Number	Date	Name	Class	Subclass	Filing Date If Appropriate
	AA						
	AB						
	AC						
	AD						
	AE						
	AF						
	AG						
	AH						
	AI						
	AJ						
	AK						

RECEIVED  
 AUG - 4 2003  
 TECHNICAL CENTER 2800

## FOREIGN PATENT DOCUMENTS

		Document Number	Date	Country	Class	Subclass	Translation	
							Yes	No
	AL							
	AM							
	AN							
	AO							
	AP							

## OTHER REFERENCES (including Author, Title, Date, Pertinent Pages, Etc.)

	AR		Wolf, Ph.D., Stanley. "Silicon Processing for the VLSI Era - Volume 2: Process Integration," ©1990 Lattice Press, pages 212-213.
	AS		
	AT		

EXAMINER

DATE CONSIDERED

\*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.